

539,337

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
8 July 2004 (08.07.2004)

PCT

(10) International Publication Number
WO 2004/057487 A2

(51) International Patent Classification⁷: **G06F 15/80**

Matthew [GB/GB]; Studio Apartment, 34 Belvedere,
Lansdown, Bath BA1 5HR (GB). **DEALTRY, Roger,**
Paul [GB/GB]; 13 Belmont, Bath BA1 5HR (GB).

(21) International Application Number:
PCT/GB2003/005451

(22) International Filing Date:
12 December 2003 (12.12.2003)

(74) Agent: **O'CONNELL, David, Christopher;** Haseltine
Lake, Imperial House, 15-19 Kingsway, London WC2B
6UD (US).

(25) Filing Language: English

(81) Designated State (*national*): US.

(26) Publication Language: English

(84) Designated States (*regional*): European patent (AT, BE,
BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU,
IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR).

(30) Priority Data:
0229788.5 20 December 2002 (20.12.2002) GB

(71) Applicant (*for all designated States except US*): **PIC-
OCHIP DESIGNS LIMITED** [GB/GB]; Second Floor
Suite, Riverside Buildings, 108 Walcot Street, Bath BA1
5GB (GB).

Published:

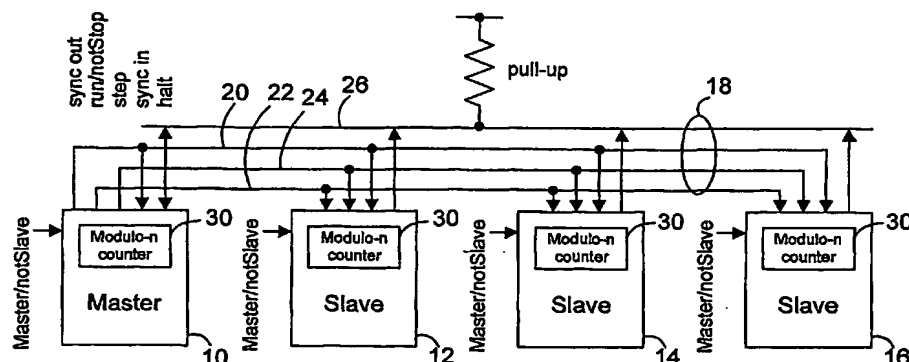
— *without international search report and to be republished
upon receipt of that report*

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **NOLAN, John,**

*For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: ARRAY SYNCHRONISATION



(57) Abstract: A method is disclosed for achieving synchronization in an array of semi-synchronous devices. A processor array has an array of processor elements, wherein each of said processor elements comprises a cycle counter, and a master processor element is able to transmit control command signals to each of the other processor elements. Each processor element is such that, on receipt of a control command signal, it acts on that signal only when its cycle counter reaches a predetermined value, and the master processor element is such that it transmits control command signals only when its cycle counter takes a value which is within a predetermined range, or "safe window". By appropriate setting of the "safe window", it can be guaranteed that, when the master processor element transmits a control command signal to each of the other processor elements, those command control signals are acted upon at corresponding times within the other processor elements.

WO 2004/057487 A2